ULTRATHIN FORM FACTOR MEMS MICROPHONES AND MICROSPEAKERS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation in part of U.S. application serial no. 10/701,860 entitled Ultrathin Form Factor MEMS Microphones and Microspeakers, filed on November 5, 2003.

BACKGROUND

[0002] The present disclosure is directed generally to micro-electro-mechanical systems (MEMS) devices and, more particularly, to processing techniques for forming ultrathin devices.

[0003] The ability to form moving parts measured in microns has opened up a huge range of applications. Such moving parts typically take the form of a beam or mesh that may form, for example, a variable capacitor, switch, or other component. The recent ability to seal micro-machined meshes has lead to the fabrication of microphones and microspeakers. See, for example, International Publication No. WO/01/20948 A2 published 22 March 2001, entitled MEMS Digital-to-Acoustic Transducer With Error Cancellation, the entirety of which is hereby incorporated by reference.

[0004] A sealed mesh can function as a movable plate of a variable capacitor, and therefore can operate as a microspeaker or microphone. For a sealed mesh to operate as a microspeaker or microphone, the device needs to be able to push air to create a soundwave just as its larger counterparts must push air to create soundwaves. For example, traditional speaker enclosures have a port on the back to allow the speaker to move freely. In the case of a microspeaker or microphone, if the chamber beneath the sealed mesh does not have a vent or other opening to ambient, movement of the sealed mesh inward is inhibited by the inability to compress the air in the chamber while movement of the mesh outward is inhibited by formation of a vacuum. Thus it is necessary to form a vent in the chamber.

[0005] Currently, such vents are formed by boring through the substrate from the rear. That requires patterning the back side of the substrate followed by an etch through the entirety of the substrate to reach the chamber. Forming of vents by this technique is slow in that several hundred microns of substrate may need to be etched to reach the

chamber beneath the sealed mesh and the diameter of the vent is small compared to its depth. Additionally, there are registration problems in that it is necessary to work from the back side of the substrate where there are no landmarks, and hundreds of microns may need to be etched to reach a chamber that may measure in the tens of microns.

[0006] U.S. patent application serial no. 10/349,618 entitled Process for Forming and Acoustically Connecting Structures on a Substrate, filed January 23, 2003 discloses a processes in which the substrate is etched in the area of the mesh. Although that represents an improvement over the prior art, the need still exists for an easy, repeatable, fast process for forming vents in the chambers of sealed meshes that are to function as speakers or microphones.

BRIEF SUMMARY

[0007] The present disclosure is directed to a CMOS process of fabricating a plurality of devices containing MEMS membranes (sealed micro-machined meshes) which begins with certain process steps being performed from the top side of a substrate carrying the plurality of devices. A carrier wafer is attached to the top side of the substrate. The thickness of the substrate is reduced using any known technique. The fabrication process is continued by performing various process steps from the back side of the substrate.

[0008] The present disclosure is also directed to a CMOS process of fabricating a plurality of devices containing MEMS membranes which begins with attaching a carrier wafer to a top side of a substrate carrying the plurality of devices. The thickness of the substrate is reduced. Process steps are then performed from the back side of the substrate. A carrier wafer is attached to the back side of the substrate and the carrier wafer on the top side of the substrate is removed. Thereafter, process steps are performed from the top side of the substrate.

[0009] This disclosure encompasses a process for fabricating a MEMS device in which the thickness of a substrate is reduced; a carrier wafer is attached to one of the top side and back side of the substrate during at least a part of the process of fabricating the MEMS device. The use of the carrier wafer may include a carrier wafer attached to the top side of the substrate to enable at least certain process steps to be performed from the back side of the substrate and/or use of a carrier wafer attached

to the back side of the substrate to enable at least certain process steps to be performed from the top side of the substrate.

[0010] As the various embodiments of the disclosure indicate, the use of carrier wafers to support the thinned wafer enables process steps to be carried out on the side opposite from the side having the carrier wafer. As the different embodiments indicate, the side carrying the carrier wafer can be varied throughout the process. Those advantages and benefits, and others, will be apparent from the description appearing below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] For the present disclosure to be easily understood and readily practiced, the present disclosure will now be described, for purposes of illustration and not limitation, in conjunction with the following figures, wherein:

[0012] FIG. 1 illustrates a substrate having a plurality of metal layers patterned to form a device;

[0013] FIG. 2 illustrates the substrate of FIG. 1 after the thickness of the substrate has been reduced;

[0014] FIG. 3 illustrates the substrate of FIG. 2 after a carrier wafer has been attached to the back side of the substrate;

[0015] FIG. 4 illustrates the substrate of FIG. 3 after the top side has been patterned with a resist;

[0016] FIG. 5 illustrates the fabrication of the mesh as a result of an anisotropic etch;

[0017] FIG. 6 illustrates the substrate of FIG. 5 after the top side has been patterned with a resist;

[0018] FIG. 7 illustrates the formation of pilot openings using a portion of the mesh as an etch mask;

[0019] FIG. 8 illustrates the substrate of FIG. 7 after the mesh has been released and the pilot openings expanded to form vent holes;

[0020] FIG. 9 illustrates how a plurality of devices may be singulated by etching either as a separate step or in conjunction with a through-wafer vent hole etch process;

[0021] FIG. 10 illustrates how a plurality of devices may be singulated using conventional dicing;

[0022] FIG. 11 illustrates the substrate of FIG. 1 after the top side has been patterned with a resist;

[0023] FIG. 12 illustrates the fabrication of the mesh as a result of an anisotropic etch;

[0024] FIG. 13 illustrates the substrate of FIG. 12 after the top side has been covered with a protective layer;

[0025] FIG. 14 illustrates the substrate of FIG. 13 after the thickness of the substrate has been reduced;

[0026] FIG. 15 illustrates the substrate of FIG. 14 after a carrier wafer has been attached to the back side of the substrate and the protective layer has been removed from the top side of the substrate;

[0027] FIG. 16 illustrates the substrate of FIG. 15 after a layer of resist has been deposited and patterned to enable certain portions of the mesh to act as an etch mask for pilot openings to be formed in the substrate;

[0028] FIG. 17 illustrates the substrate of FIG. 16 after pilot openings have been formed as a result of an anisotropic etch;

[0029] FIG. 18 illustrates the substrate of FIG. 17 after the mesh has been released and the pilot openings expanded to form vent holes;

[0030] FIG. 19 illustrates the substrate of FIG. 5 after a second carrier wafer has been attached to the top side of the substrate; a protective material may fill gaps between carrier wafer and substrate;

[0031] FIG. 20 illustrates the substrate of FIG. 19 after the first carrier wafer has been removed from the back side of the substrate;

[0032] FIG. 21 illustrates the substrate of FIG. 20 after a layer of resist has been deposited and patterned on the back side of the substrate;

[0033] FIG. 22 illustrates the substrate of FIG. 21 after the formation of vent holes;

[0034] FIG. 23 illustrates the substrate of FIG. 22 after the attachment of a third carrier wafer to the back side of the substrate;

[0035] FIG. 24 illustrates the substrate of FIG. 23 after the second carrier has been removed from the top side of the substrate; the protective layer has also been removed.

[0036] FIG. 25 illustrates the substrate of FIG. 24 after the mesh has been released;

[0037] FIG. 26 illustrates the substrate of FIG. 5 after an isotropic etch has been performed to release the mesh;

[0038] FIG. 27 illustrates the substrate of FIG. 26 after a second carrier wafer has been attached to the top side of the substrate;

[0039] FIG. 28 illustrates the substrate of FIG. 27 after the first carrier wafer has been removed from the back side of the substrate;

[0040] FIG. 29 illustrates the substrate of FIG. 28 after a layer of resist has been patterned;

[0041] FIG. 30 illustrates the substrate of FIG. 29 after an etch has been performed to form vent holes;

[0042] FIG. 31 illustrates the substrate of FIG. 4 after the attachment of a second carrier wafer to the top side of the substrate and the removal of the first carrier wafer from the back side of the substrate; a protective layer may fill gaps between carrier wafer and substrate.

[0043] FIG. 32 illustrates the substrate of FIG. 31 after a layer of resist has been patterned on the back side of the substrate;

[0044] FIG. 33 illustrates the substrate of FIG. 32 after the formation of vent holes;

[0045] FIG. 34 illustrates the substrate of FIG. 33 with the remaining resist removed;

[0046] FIG. 35 illustrates the substrate of FIG. 34 after the attachment of a third carrier wafer to the back side of the substrate;

[0047] FIG. 36 illustrates the substrate of FIG. 35 after the removal of the second carrier wafer from the top side of the substrate;

[0048] FIG. 37 illustrates the fabrication of the mesh as a result of an anisotropic etch;

[0049] FIG. 38 illustrates the substrate of FIG. 37 after the mesh is released;

[0050] FIG. 39 illustrates the substrate of FIG. 1 after a layer of resist has been formed and patterned;

[0051] FIG. 40 illustrates the substrate of FIG. 39 after a carrier wafer has been attached to the top side of the substrate;

[0052] FIG. 41 illustrates the substrate of FIG. 40 after the substrate has been thinned;

[0053] FIG. 42 illustrates the substrate of FIG. 41 after a layer of resist has been formed and patterned on the back side of the substrate;

[0054] FIG. 43 illustrates the substrate of FIG. 42 after the formation of vent holes;

[0055] FIG. 44 illustrates the substrate of FIG. 43 after the resist has been removed;

[0056] FIG. 45 illustrates the substrate of FIG. 44 after a carrier wafer has been attached to the back side of the substrate;

[0057] FIG. 46 illustrates the substrate of FIG. 45 after the carrier wafer on the top side of the substrate has been removed;

[0058] FIG. 47 illustrates the fabrication of the mesh as a result of an anisotropic etch;

[0059] FIG. 48 illustrates the substrate of FIG. 47 after the mesh is released;

[0060] FIG. 49 illustrates the substrate of FIG. 1 after a layer of resist has been formed and patterned:

[0061] FIG. 50 illustrates the fabrication of the mesh on the substrate of FIG. 49 as a result of an anisotropic etch;

[0062] FIG. 51 illustrates the attachment of a carrier wafer to the top side of the substrate of FIG. 50 through the application of an adhesive layer with or without a cushion material interposed between the substrate and the carrier wafer;

[0063] FIG. 52 illustrates the substrate of FIG. 51 after the thickness of the substrate has been reduced;

[0064] FIG. 53 illustrates the substrate of FIG. 52 after a layer of resist has been formed and patterned on the back side of the substrate;

[0065] FIG. 54 illustrates the substrate of FIG. 53 after the formation of vent holes;

[0066] FIG. 55 illustrates the substrate of FIG. 54 after the resist has been removed;

[0067] FIG. 56 illustrates the substrate of FIG. 55 after a carrier wafer has been attached to the back side of the substrate;

[0068] FIG. 57 illustrates the substrate of FIG. 56 after the carrier wafer on the top side of the substrate has been removed; and

[0069] FIG. 58 illustrates the substrate of FIG. 57 after the mesh is released.

DETAILED DESCRIPTION

[0070] A first embodiment of the present disclosure is illustrated in conjunction with FIGs. 1 – 9. In FIG. 1, a wafer 10 (a portion of which is seen in FIG. 1) is received from a CMOS foundry. Those of ordinary skill in the art will recognize the wafer carries a plurality of devices, one of which is shown in FIG. 1. At the CMOS foundry, a silicon substrate 12 has been processed so as to form alternating layers of, for example, a dielectric material and a metal. The wafer 10 illustrated in FIG. 1 has a first layer of dielectric material 14 carrying a first metal layer 16. The first metal layer 16 has been patterned such that a portion thereof forms a micro-machined mesh 18. Formed on the first metal layer 16 is a second layer of dielectric 20. The second layer

of dielectric 20 carries a second metal layer 22 which has been patterned to have an opening 24 formed therein. The second metal layer 22 carries a third layer of dielectric 26. The third layer of dielectric 26 carries a third layer of metal 28 which has been patterned to have an opening 30 formed therein. A top layer of dielectric 32 is formed on top of the third metal layer 28.

[0071] The present disclosure is not limited to the position and configuration of the metal layers shown in the figures. For example, the pattern shown in FIG. 1 could be implemented in metal layers two, three and four such that references herein to a first, second and third layers of metal need not correspond to metal layers one, two and three, respectively. Additionally, the configuration of the layers of metal need not be as shown in the figures but rather may vary depending upon the device to be fabricated.

[0072] As previously mentioned, the wafer 10 would be received, for example, as shown in FIG. 1 from the CMOS foundry. Thereafter, the wafer 10 will be subjected to post-processing fabrication steps. Although it is anticipated that the post-processing fabrication steps will take place in a facility different from the CMOS foundry which fabricated the wafer 10, that is not a requirement of the present disclosure.

[0073] Turning to FIG. 2, a CMP process, back side grinding, a reactive ion etch (RIE) a dry, reactive ion etch (DRIE) or other process is performed on the back side of the wafer 10 to thin the wafer to 50 – 100 μm. Depending on the process selected for thinning the wafer, it may necessary to take steps to protect the top side of the wafer.

[0074] Turning to FIG. 3, a layer of adhesive 34 is used to attach a first carrier wafer 36 to the back side of the substrate 14. Openings (not shown) may be provided in the carrier wafer 36 and/or adhesive layer 34 to provide for cooling of the substrate 12. Additionally, those of ordinary skill in the art will recognize that, depending on the amount of substrate 14 being removed and the process being performed, it may be necessary to attach a temporary carrier wafer (not shown) to the top side of wafer 10 to provide support for the thinning process. If such a temporary support is needed, it is removed after first carrier wafer 36 is attached as shown in FIG. 3.

[0075] FIG. 4 illustrates the substrate 12 of FIG. 3 after a layer of resist 38 is formed (by any appropriate process) on the top side and patterned (by any appropriate process) to provide an opening 40 in the area of the mesh 18. In FIG. 5, the substrate 12 of FIG. 4 is illustrated being subjected to an anisotropic etch through the dielectric layers

32, 26, 20 and 14 to form the mesh. The patterned resist 38 and the first metal layer 16 are used to pattern the first dielectric layer 14. The layer of resist 38 may not be necessary if it is not necessary to protect the top layer of dielectric 32.

[0076] FIG. 6 illustrates the substrate of FIG. 5 after the top side has been patterned with a layer of resist 42 to enable certain portions of the mesh 18 to act as an etch mask for pilot openings to be formed in the substrate 12. FIG. 7 illustrates the substrate 12 of FIG. 6 being subjected to a DRIE anisotropic etch which forms pilot openings 44 extending through the silicon substrate 12 and stopping at the layer of adhesive 34.

[0077] FIG. 8 illustrates the substrate 12 being subjected to an isotropic etch so as to release the mesh 18 from the substrate 12 by removal of the substrate material from under the mesh 18. Other forms of releasing the mesh could be provided, such as removal of a sacrificial layer (not shown). As the mesh 18 is being released, the pilot openings 44 are being expanded to form vent holes 46. Because the vent holes 46 are formed by enlarging the pilot openings 44, and the pilot openings 44 are formed by using a portion of the mesh 18 as an etch mask, the vent openings 46 will be in alignment under the released mesh 18.

[0078] FIG 9 illustrates a larger portion of the wafer 10 such that two adjacent devices carried by substrate 12 are illustrated. FIG 9 illustrates how a plurality of devices may be singulated by etching. The etching may be performed either as a separate step or in conjunction with the step of releasing the mesh 18 and/or forming vent holes 46 as illustrated in FIG 8. In FIG 9, it is seen that adjacent devices are laid out with a gap of approximately 10 μm between adjacent devices, although the gap can be varied by design, from a couple of microns to a couple of hundred microns. The layer of resist 38 is patterned such that while the mesh 18 is being released and the vent holes 46 are being formed, adjacent devices are being singulated. Alternatively, this singulation process could be performed separately, assuming an appropriate layer of resist was formed and patterned. However, because the releasing of the mesh 18 and formation of vent holes 46 is a through-wafer etch process, the singulation of the devices into separate chips can be completed at the same time. Thereafter, the adhesive layer can be de-adhered by heat, UV light or other means enabling each device (chip) to be picked up individually and packaged.

[0079] FIG. 10 illustrates how the wafer 10 may be singulated using a dicing saw as is known in the art. Because the dicing saw provides a cut of a approximately 65 μm, adjacent devices will likely be laid out with a spacing of 100 - 200 μm between adjacent devices. Such a spacing allows for dicing saws of different thicknesses to be used while ensuring that the devices are not harmed. After dicing with a dicing saw, the adhesive layer can be de-adhered thus leaving the individual chips to be picked up and packaged.

[0080] FIGs. 11 – 18 illustrate another embodiment of the present disclosure. The embodiment of FIG. 11 – 18 is similar to the first embodiment, except that the thinning of the wafer 10 occurs at a different point in the process. The process of FIGs. 11 – 18 begins with a wafer 10 of the type shown in FIG. 1. FIG. 11 illustrates the wafer 10 of FIG. 1 after the top side has been patterned with a resist 50.

[0081] Turning to FIG. 12, the substrate 12 of FIG. 11 is illustrated being subjected to an anisotropic etch through the dielectric layers 32, 26, 20 and 14. The patterned resist 50 and the first metal layer 16 are used to pattern the first dielectric layer 14 and to form mesh 18. The layer of resist 50 may not be necessary if it is not necessary to protect the top layer of dielectric 32. In FIG. 13, a protective layer of resist 52 is formed on the top side of wafer 10.

[0082] In FIG. 14, a CMP process, back side grinding, RIE, DRIE or other process is performed on the back side of the wafer 10 to thin the wafer to 50 – 100 μm. In FIG. 15, a layer of adhesive 34 is used to attach the first carrier wafer 36 to the back side of the substrate 14. Openings (not shown) may be provided in the first carrier wafer 36 and/or adhesive layer 34 to provide for cooling of the substrate 12. Additionally, those of ordinary skill in the art will recognize that, depending on the amount of substrate 14 being removed and the process being performed, it may be necessary to attach a temporary carrier wafer (not shown) to the top side of wafer 10 to provide support for the thinning process. If such a temporary support is needed, it is removed after first carrier wafer 36 is attached as shown in FIG. 15.

[0083] The process continues as shown in FIG. 16 – 18 which are the same as FIGs. 6 – 8, respectively. Thereafter, singulation may be performed using either the method of FIG. 9 or FIG. 10.

[0084] Another embodiment is illustrated in conjunction with FIGs. 1 – 5 and 19 – 25. In this embodiment, the process as discussed in conjunction with FIGs. 1 –5 is carried

out as discussed above. However, upon forming the mesh 18 as shown in FIG. 5, the process continues as shown in FIG. 19. In FIG. 19, the wafer 10 is bonded via a layer of adhesive 54 to a second carrier wafer 56 on the top side of the wafer 10. The resist 38 illustrated in FIG. 5 may or may not be removed before the bonding step. Thereafter, as shown in FIG. 20, the first carrier wafer 36 is detached from the wafer 10 using any method appropriating for de-adhering layer 34.

[0085] Turning now to FIG. 21, a layer of resist 60 is formed and patterned to provide openings for fabrication of the vent holes. Those of ordinary skill in the art will realize that landmarks from the top side of the wafer 10 need to be transferred to the back side to provide landmarks for registration of the mask needed to pattern the layer of resist 60. Transferring such landmarks is known in the art and therefore not described herein. After the layer of resist 60 has been patterned, the wafer 10 is subjected to RIE or DRIE as shown in FIG. 22 to fabricate vent holes 46.

[0086] In FIG. 23, the wafer 10 is bonded to a third carrier wafer 66 with a layer of adhesive 64. The resist from the previous step may be removed by any appropriate means, such as oxygen plasma cleaning. The second carrier wafer 56 is detached from the wafer 10 by de-adhering the layer of adhesive 54 resulting in the structure illustrated in FIG. 24. Any protective layers that have been provided can be removed by appropriate methods. An isotropic etch of the silicon substrate 12 is performed to release the mesh 18 from the substrate and to further enlarge the vent holes 46. Thereafter, singulation may be performed as discussed above with either FIGs. 9 or 10.

[0087] Another embodiment is illustrated in conjunction with FIGs. 1 – 5 and 26 – 30. In this embodiment, the process as discussed above in conjunction with FIGs. 1 –5 is carried out as discussed above. However, in this embodiment, the mesh 18 is released as shown in FIG. 26 by, for example, an isotropic etch of the silicon substrate 12. The wafer 10 is bonded to the second carrier wafer 56 through the use of a layer of adhesive 54 on the top side of the wafer 10 as illustrated in FIG 27.

[0088] Turning now to FIG. 28, the first carrier wafer 36 is detached from the wafer 10 by de-adhering adhesive layer 34. In FIG. 29, a layer of resist 70 has been formed and patterned on the back side of the wafer 10 to provide for fabrication of the vent holes. In FIG. 30, an RIE or DRIE process is performed to fabricate the vent holes 46. The resist 70 may be stripped off at the end of the etch. Because this is a through wafer

etch process, singulation of the chips can be completed at the same time as the vent holes 46 are fabricated as discussed above in conjunction with FIG 9. Alternatively, singulation may be performed using a dicing saw as discussed above in conjunction with FIG 10.

[0089] Another embodiment is illustrated in conjunction with FIGs. 1 – 4 and 31 – 38. In this embodiment, the process as discussed above in conjunction with FIGs. 1 –4 is carried out as discussed above. After the wafer 10 has been processed as shown in FIG. 4, the wafer 10 is bonded to the second carrier wafer 56, using a layer of resist 54 and the first carrier wafer 36 is removed by de-adhering the layer of adhesive 34 resulting in the structure illustrated in FIG. 31.

[0090] In FIG. 32, the back side of the wafer 10 has a layer of resist 72 formed and patterned as shown in the figure. An RIE or DRIE is performed as shown in FIG. 33 to fabricate the vent holes 46. The resist 72 on the back side of the wafer is then removed as shown in FIG. 34.

[0091] Turning now to FIG. 35, the third carrier wafer 66 is bonded to the back side of wafer 10 with a layer of adhesive 64. In FIG. 36, the second carrier wafer 56 is removed from the wafer 10 by de-adhering the layer of adhesive 54. In FIG. 37, an isotropic etch through the dielectric layers 32, 26, 20 and 14 is performed to form the mesh 18. In FIG. 38, an isotropic etch of the silicon substrate 12 is performed to release the mesh 18 and to enlarge the vent holes 46. Because this is a through-wafer etch process, the separation of the chips can be completed at the same time as discussed above in conjunction with FIG. 9. Alternatively, because of the carrier wafer, singulation can be performed before the device is completely fabricated by taking advantage of any through-wafer etch processes. For example, singulation could occur along with the etching of the substrate shown in FIG. 34. As another alternative, the wafer 10 can be diced with a dicing saw as discussed above in conjunction with FIG. 10.

[0092] Completing the process, the mesh 18 of any of the embodiments may be sealed using known deposition techniques to form a membrane capable of operating as a speaker or a microphone.

[0093] FIG. 1 and FIGs. 39 – 48 illustrate another embodiment of the present invention. FIG. 39 illustrates the substrate of FIG. 1 after a layer of resist 76 has been formed and patterned. The reader will understand that the layer of resist may be

formed and patterned latter in the process, or eliminated altogether, as will be noted later. FIG. 40 illustrates the substrate of FIG. 39 after the carrier wafer 56 is attached to the substrate with the adhesive layer 54, which may include optional cushion material. Carrier wafer 56 has been previously identified as the second carrier wafer, although in this embodiment it is the first carrier wafer connected to the substrate.

[0094] Fig. 41 illustrates the substrate of FIG. 40 after the substrate has been thinned (reduced in thickness) using any known method, including those previously described. FIG. 42 illustrates the substrate of FIG. 41 after a layer of resist 82 has been formed and patterned. Thereafter, and as shown in FIG. 43, the substrate is subjected to an anisotropic etch process to fabricate vent holes 46. Thereafter, as shown in FIG. 44, resist 82 is removed.

[0095] FIG. 45 illustrates the attachment of the carrier wafer 36 to the substrate through the use of adhesive layer 34. In this embodiment, the carrier wafer 36 is the second carrier wafer to be attached to the substrate. The carrier wafer 56 and adhesive layer 54 are then removed as shown in FIG. 46. If the layer of resist 76 has not been previously formed, it may be formed and patterned at this time. If it is not necessary to protect the top layer of dielectric 32, the layer of resist 76 may be eliminated.

[0096] FIG. 47 illustrates the substrate 12 being subjected to an anisotropic etch through dielectric layers 32, 26, 20 and 14 to form the mesh 18. FIG. 48 illustrates the substrate of FIG. 47 being subjected to an isotropic etch so as to release the mesh 18 from the substrate 12 by removal of the substrate material from under the mesh 18. Other forms of releasing the mesh 18 could be provided, such as removal of a sacrificial layer (not shown). Once the mesh 18 is released, the plurality of devices carried by the substrate may be singulated, either before or after sealing of the mesh 18 to form a membrane.

[0097] FIG. 1 and FIGs. 49 – 58 illustrate another embodiment of the present invention. FIG. 49 illustrates the substrate of FIG. 1 after a layer of resist 76 has been formed and patterned. The reader will understand that the layer of resist 76 may be formed and patterned latter in the process, or eliminated altogether, as previously described.

[0098] FIG. 50 illustrates the substrate 12 being subjected to an anisotropic etch through dielectric layers 32, 26, 20 and 14 to form the mesh 18. FIG. 51 illustrates

the carrier wafer 56 attached to the substrate with the adhesive layer 54, which may include optional cushion material. Thereafter, as shown in FIG. 52, the substrate is thinned (reduced in thickness) using any known method, including those previously described. FIG. 53 illustrates the substrate of FIG. 52 after a layer of resist 82 has been formed and patterned on the back side. Thereafter, and as shown in FIG. 54, the substrate is subjected to an anisotropic etch process to fabricate vent holes 46. Thereafter, as shown in FIG. 55, resist 82 is removed.

[0099] FIG. 56 illustrates the substrate of FIG. 55 after the carrier wafer 36 has been attached to the back side of the substrate using the adhesive layer 34. The carrier wafer 56 is then removed along with the layer of adhesive 54 as shown in FIG. 57. If the layer of resist 76 has not been previously formed, it may be formed and patterned at this time. If it is not necessary to protect the top layer of dielectric 32, the layer of resist 76 may be eliminated.

[00100] FIG. 58 illustrates the substrate of FIG. 57 being subjected to an isotropic etch so as to release the mesh 18 from the substrate 12 by removal of the substrate material from under the mesh 18. Other forms of releasing the mesh 18 could be provided, such as removal of a sacrificial layer (not shown). Once the mesh 18 is released, the plurality of devices carried by the substrate may be singulated, either before or after sealing of the mesh 18 to form a membrane.

[00101] This disclosure describes a simplified process for making vent holes while eliminating the need for acoustic cavities in each chip for a CMOS MEMS based microphone or microspeaker. Certain of the disclosed embodiments are performed entirely from the top side of the wafer thereby eliminating the need for back side alignment of vent holes relative to the mesh. By reducing the wafer thickness to a specified thickness with standard processes, which are capable of achieving well controlled uniformity across the wafer, the length of the vent holes can be well defined. Therefore, the etch time of a vent hole can be well defined and optimized. Moreover, instead of using special and expensive techniques to etch deep, narrow vent holes, standard RIE techniques can be used to etch the vent holes. This allows for the post-CMOS production to be transferred into a standard CMOS foundry. By integrating chip dicing with the post-CMOS process, manufacturing costs associated with the dicing and separation process can be reduced. By integrating chip dicing with

the post-CMOS process, the extra chip size required for dicing with traditional dicing saws may be eliminated.

[00102] While the present disclosure has been described in connection with preferred embodiments thereof, those of ordinary skill in the art will recognize that many modifications and variations are possible. The present disclosure is intended to be limited only by the following claims and not by the foregoing description which is intended to set forth the presently preferred embodiments.